ELECTRONIC DEVICES

PRACTICE QUESTIONS (Pg. 14)

8) Pure Si at 300 K has equal electron (n_e) and hole (n_h) concentrations of 1.5×10^{16} m^{-3}. Doping by indium increases n_h to 4.5×10^{22} m^{-3}. Calculate n_e in the doped Si.

SOL: For a doped semiconductor, we have $n_e\, n_h = n_i^2$

where n_i is intrinsic concentration in a pure semiconductor.

Here $n_h = 4.5 \times 10^{22}$ m^{-3} and $n_i = 1.5 \times 10^{16}$ m^{-3}.

$$\therefore \quad n_e = \frac{n_i^2}{n_h} = \frac{(1.5 \times 10^{16}\ \text{m}^{-3})^2}{4.5 \times 10^{22}\ \text{m}^{-3}} = \mathbf{5.0 \times 10^{9}\ m^{-3}}.$$

9) A semiconductor has equal electron and hole concentrations of 2×10^8 / m^3. On doping with a certain impurity, the hole concentration increases to 4×10^{10} / m^3. (i) What type of semiconductor is obtained on doping ? (ii) Calculate the new electron concentration of the semiconductor. (iii) How does the energy gap vary with doping ?

SOL: (i) p-type, because on doping, the hole concentration increases.

(ii) For a doped semiconductor, we have $n_e\, n_h = n_i^2$

$$\therefore \quad n_e = \frac{n_i^2}{n_h} = \frac{[2 \times 10^8\ /\ \text{m}^3]^2}{4 \times 10^{10}\ /\ \text{m}^3} = \mathbf{10^6\ /\ m^3}.$$

(iii) Energy gap decreases with doping.

10) The number of electron-hole pairs in an intrinsic semiconductor is 2×10^{19} /m^3 at 27°C. If this semiconductor is doped by a donor impurity such that the number of conduction electrons becomes 2×10^{24} /m^3, calculate the number of holes at 27°C. Also calculate the dopant concentration.

SOL: For doped semiconductor , we have $n_e\, n_h = n_i^2$

Given : $n_e = 2 \times 10^{24}$ m^{-3} and $n_i = 2 \times 10^{19}$ m^{-3}.

$$\therefore \quad n_h = \frac{n_i^2}{n_e} = \frac{(2 \times 10^{19}\ \text{m}^{-3})^2}{2 \times 10^{24}\ \text{m}^{-3}} = \mathbf{2 \times 10^{14}\ m^{-3}}.$$

It has become an *n*-type semiconductor.

$$\therefore \text{ dopant concentration, } N_D = n_e = \mathbf{2 \times 10^{24}\ m^{-3}}.$$

11) The electrical conductivity of a semiconductor increases when electromagnetic radiation of wavelength shorter than 2480 nm is incident on it. Find the band gap for the semiconductor. Given : h = 6.63 × 10^{-34} Js, c = 3.0 × 10^8 m s^{-1} and 1 eV = 1.6 × 10 ^{19}J.

SOL: The band gap is the minimum energy required to push an electron from the valance band into the conduction of the semiconductor, that is,

$$\Delta E = \frac{hc}{\lambda} = \frac{(6.63 \times 10^{-34}\ \text{J s}) \times (3.0 \times 10^{8}\ \text{m s}^{-1})}{2480 \times 10^{-9}\ \text{m}}$$

$$= 8.02 \times 10^{-20}\ \text{J} = \frac{8.02 \times 10^{-20}\ \text{J}}{1.6 \times 10^{-19}\ \text{J/eV}} \simeq \mathbf{0.5\ eV}.$$

12) What is meant by the term 'doping' of an intrinsic semiconductor ? How does it affect the conductivity of a semiconductor ?

SOL: It is a process of adding impurity to an intrinsic semiconductor in a controlled manner. Doping creates more free electrons and holes in a semiconductor. So it increases the conductivity of the semiconductor significantly and the semiconductor becomes an extrinsic

semiconductor.

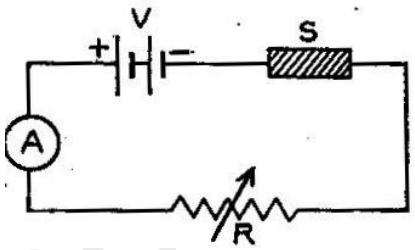
13) How does the energy gap in an intrinsic semiconductor vary , when doped with a pentavalent impurities?

SOL: Energy gap decreases

14) How does the forbidden energy gap of an intrinsic semiconductor vary with increase in temperature?

SOL: It does not changes.

15) The diagram shows a piece of pure semiconductor *S* in series with a variable resistor *R* and a source of constant voltage V .Would you increase or decrease the value of *R* to keep the reading of ammeter (A) constant, when semiconductor *S* is heated ? Give reason.



SOL: When the semiconductor *S* is heated, its resistance decreases. Hence, to keep the current in the circuit constant, the resistance ***R*** would have to be increased.

16) (i) Is the ratio of number of holes and number of conduction electrons in n-type extrinsic semiconductor more than, less or equal to 1? (ii) what in p-type semiconductor?

SOL: (i) less than 1 (ii) more than 1.

17) **In a semiconductor, the concentration of electrons is 8×10^{13} cm $^{-3}$ and that of holes is 5×10^{12} cm^{-3}. Is it a p-type or n-type semiconductor.**

Ans: n-type semiconductor.

18) **A semiconductor has equal electron and hole concentrations of 6×10^{8} m^{-3} . On doping with a certain impurity, electron concentration increases to 8×10^{12} m^{-3}. Identify the type of semiconductor after doping.**

Ans: n-type.

19) **A semiconductor has equal electron and hole concentrations of 6×10^{5}/m^{3}. On doping with certain impurity, electron concentration increases to 9×10^{12}/m^{3}. (i) Identify the new semiconductor obtained after doping, (ii) Calculate the new hole concentration.**

Ans. (i) n-type, because on doping electron concentration increases. (ii) 4×10^{4}/m^{3}.

20) What are energy bands ? How are they formed ? Distinguish between conductors (metals), insulators and semiconductors on the basis of their energy band diagrams.

21) Explain the formation of energy bands in solids. Draw energy band diagram for (i) a conductor, (ii) an intrinsic semiconductor.

22) Explain how an intrinsic semiconductor can be converted into (i) n -type, (ii) p -type semiconductor. Give one example of each and draw their energy band diagrams.

23) How is a p-type semiconductor formed ? Name the major charge carriers in it. Draw energy band diagram of a p-type semiconductor.

24) How is an n-type semiconductor formed ? What type of charge carriers are there in it ? Draw energy band diagram of an n-type semiconductor.

25) What do you understand by p - and n -type semiconductors ? Distinguish between them on the basis of energy band diagram. Give the reason why a p-type semiconductor crystal is electrically neutral, although $n_h >> n_e$.

26) Deduce an expression for the conductivity of a p-type semiconductor.

PRACTICE QUESTIONS (Diode) Pg 26

1) Name the type of biasing which results in a very high resistance of a *p-n* junction diode.

ANS: Reverse biasing.

2) **How does the width of the depletion region of a *p-n* junction vary, if the reverse bias applied to it decreases ?**

Ans. It decreases.

3) What happens to the width of depletion layer of a *p -n* junction when it is
(a) forward biased?
(b) reverse biased? [All India 2011]

SOL: (a) Depletion layer's width decreases in forward bias.

(b) Depletion layer's width increases in reverse bias.

4) Why cannot we take one slab of p-type semiconductor and physically join it to another slab of n-type semiconductor to get *p -n* junction? [All India 2010C]

SOL: In this way, continuous contact cannot be produced at atomic level and junction will behave as a discontinuity for flowing charge carrier.

5) Zener diodes have higher dopant densities as compared to ordinary p-n junction diodes.. How does it affect the *(i)* Width of the depletion layer ? *(ii)* Junction field ? [S.P.]

SOL: *(i)* Width of depletion layer decreases. *(ii)* Junction field increases.

6) How is a sample of an n-type semiconductor electrically neutral though it has an excess of negative charge carriers ? [S.P.]

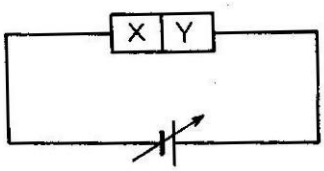
SOL: For negative charge carries in excess there are as many protons in the donor impurities in n-type of semiconductor.

7) How is forward biasing different from reverse biasing in a p-n junction diode? [Delhi 2011]

SOL:

Forward bias	**Reverse bias**
1.) Positive terminal of battery is connected to p-type and negative terminal to n-type semiconductor.	Positive terminal of battery connected to n-type and negative terminal to p-type semiconductor.
2.) Depletion layer is very thin	Depletion layer is thick.
3.) p-n junction offers very low resistance.	p-n junction offers very high resistance.
4.) An ideal diode have zero resistance	The ideal diode have infinite resistance.

8) Two semiconductor materials *X* and Y shown in the figure, are made by doping germanium crystal with indium and arsenic respectively. The two are joined end to end and connected to a battery, as shown.

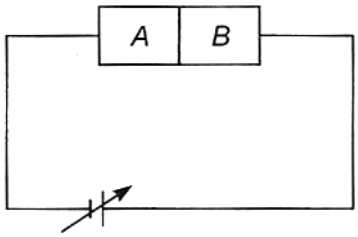


***i)* will the junction be forward biased or reverse biased ?**

***ii)* sketch a *V-i* graph for this arrangement.**

ANS: (i) *X* is p-type and Y is n-type. Thus, the junction is reverse-biased.

9) Two semiconductor materials A and *B* shown in the given figure, are made by doping germanium crystal with arsenic and indium respectively.
The two are joined end connected to a battery as shown.

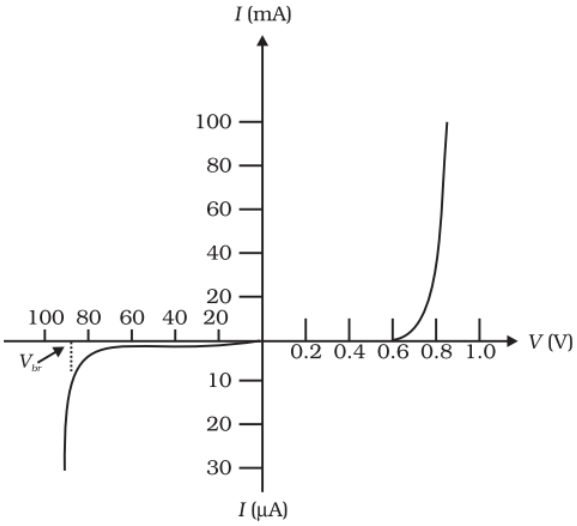


(a) Will the junction be forward biased or reverse biased?
(b) Sketch a V-I graph for this arrangement. [All India 2007]

SOL: As is pentavalent and **In** is trivalent, so they produce *n* and p-type respectively. Arsenic is pentavalent and Indium is trivalent, so on dopping Germanium with Arsenic n-type semiconductor will form.

(a) as A (n-type) is connected with negative terminal and *B* (p-type) is connected with positive terminal of the battery so the junction is in forward bias.

(b) *V-I* graph



(c)

10) Draw V-I characteristics of a *p-n* junction diode in
(i) forward bias, (ii) reverse bias. [All India 2009]

11) Draw *V-I* characteristics of a *p-n* junction diode. Answer the following questions, giving reasons:
a) Why is the current under reverse bias almost independent of the applied potential upto a **critical voltage?**
b) Why does the reverse current show a sudden increase at the critical voltage ?

Name any semiconductor device which operates under the reverse bias in the breakdown region. [All India 2013]

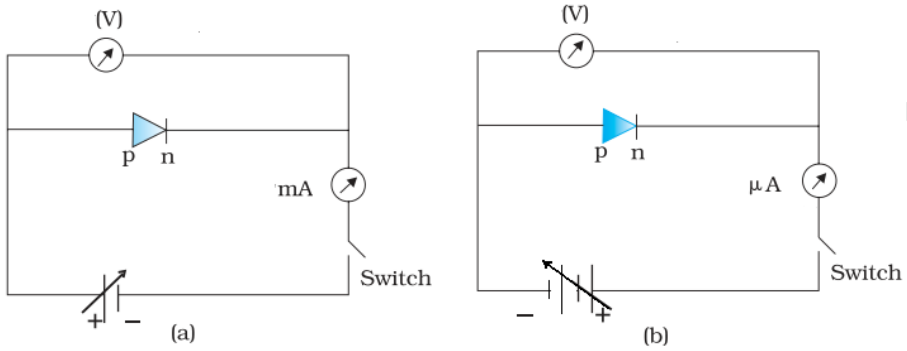
SOL: (a) **In reverse bias the junction width increases**: The higher junction potential restricts the flow of majority charge carriers. However, such a field favours flow of minority carriers. Thus, reverse bias current is due to flow of minority carriers only. Since the number of minority carriers is very small, the current is small and almost independent of the applied potential upto a critical (before breakdown) voltage.

(b) **At a critical (breakdown) voltage** the reverse bias current shows a sudden increase. Under high reverse bias, the high junction field may strip an electron from the valence band, which can tunnel to the n-side through the thin depletion layer. This mechanism of emission of electrons after a critical applied voltage leads to a high reverse (breakdown) current.

A **zener diode** operates under the reverse bias in the breakdown region.

12) Draw the circuit diagram showing how a *p-n* junction diode is (a) forward biased and (b)reverse biased. How is the width of depletion layer affected in the two cases? [All India 2011C][All India 2009]

SOL: Circuit diagram of forward biased and reverse biased *p-n* junction diode is shown below

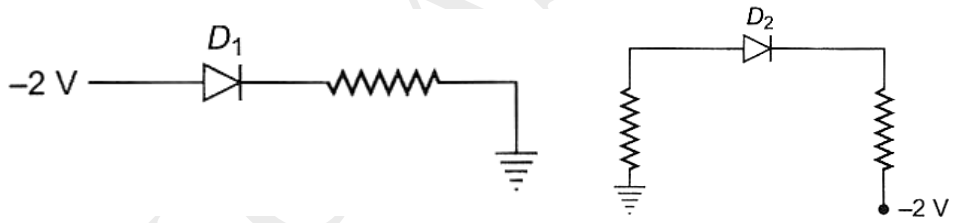


The width of depletion layer

(a) decreases in forward bias.

(b) increases in reverse bias.

13) Which one of the two diodes D_1 and D_2 in the given figure is



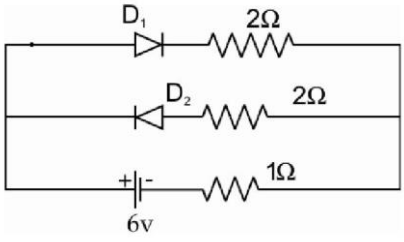
(a) forward biased?

(b) reverse biased? [2007]

SOL: D_2 is in forward bias become p-type is at higher potential (0) as compared to n-type (–2 V).

(b) D_1 is in reverse bias because p-type is a lower potential (– 2 V) as composed to n-type (0 V).

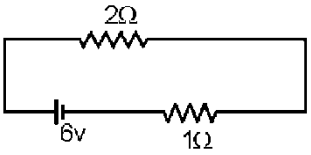
14) For the circuit shown here, find the current flowing through the 1 Ω resistor. Assume that the two diodes, D_1 and D_2, are ideal diodes.[CBSE Sample Paper 2013]



SOL: Diode D_1 is forward biased while Diode D_2 is reverse biased Hence the resistances, of (ideal) diodes, D_1 and D_2, can be taken as zero and infinity, respectively.

The given circuit can, therefore, be redrawn as shown in the figure.

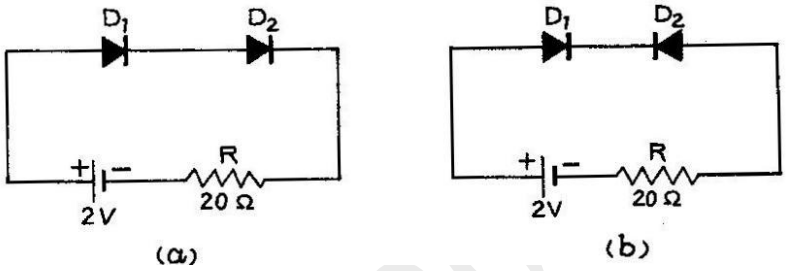
∴ Using ohm's law,



$I = \frac{6}{(2+1)} A = 2A$

∴ current flowing in the 1Ω resistor, is 2A.

15) *Find* the currents through the resistance *R* of the circuits (a) and (b), when similar diodes D_1 and D_2 are connected as shown.

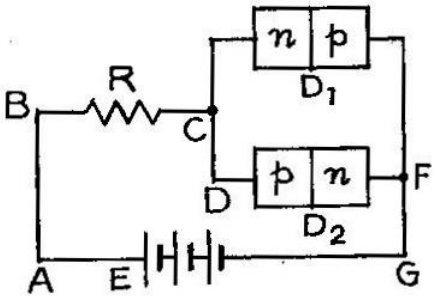


SOL: In circuit (a), both diodes are forward-biased and offer zero resistance (assuming the diodes to be ideal). Hence the current in the circuit resistance *R is*

$$I = \frac{V}{R} = \frac{2V}{20\Omega} = 0.1A$$

In circuit (b), the diode D_2 is reverse-biased and offers infinite resistance to the circuit. Hence the current in the circuit is zero.

16) The figure shows two junction diodes D_1 and D_2 along with a resistance *R* and a d.c. battery *E* . Show the path of the flow of appreciable current in the circuit.

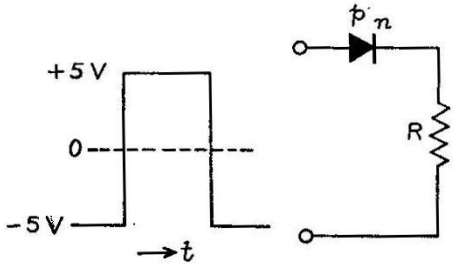


SOL: D_1 is reverse-biased, hence there is no appreciable current through it. The current path is

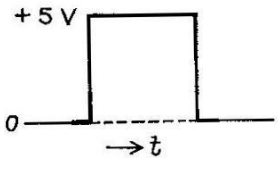
$E \rightarrow A \rightarrow B \rightarrow C \rightarrow D \rightarrow F \rightarrow G \rightarrow E.$

17) What is an ideal junction diode ?

A square wave (-5 V to + 5 V) is applied to a *p-n* junction diode, as shown in fig page. Draw the output waveform across the resistor *R.* Assume that the diode is ideal.



SOL: An ideal junction diode is one that offers zero resistance when forward-biased and infinite resistance when reverse-biased. Here, the input waveform (given square wave) is of digital nature, that is, it is either - 5 V or + 5 V. When the input is 5 V, the diode becomes reverse-biased. Therefore, so



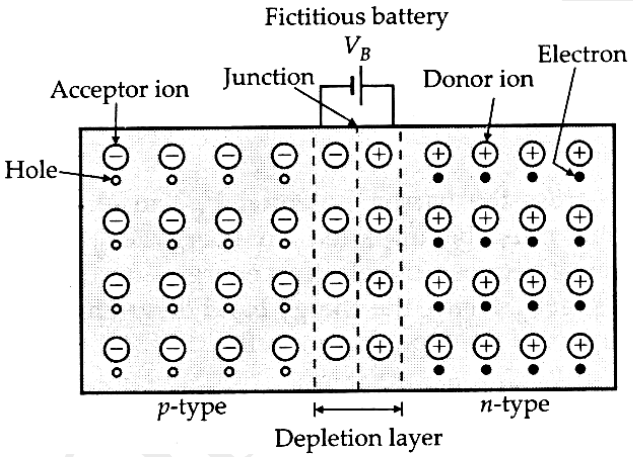
long the input remains - 5 V , no output is obtained across R . When the input becomes + 5 V , the diode becomes forward-biased and a current flows through the resistor R . As the diode is ideal, the output across R will be exactly 5 V. Thus, the output will be either 0 or + 5 V. The waveform will be as shown.

18) Explain the formation of the depletion region for a *p-n* junction.
(a) How does the width of this region change when the junction is(i) forward biased and (ii) reverse biased.
(b) How does an increase in the doping concentration affect the width of the depletion region?[CBSE Sample Papers 2013]

SOL: Formations of depletion region: When a p-type semiconductor is joined with an n-type semiconductor diffusion of charge carrier take place across the junction. The p-type holes are minority carriers. So, they diffuse towards n-type, where they are in majority. In same way, the n-type electrons are majority carriers, so they diffuse towards p-type where they are in minority. In both cases, when an electron meets a hole, then they cancel the effect of each other.

Then, a thin layer is formed at the junction which becomes depleted (free) of the mobile charge carriers and has only immotile ions. This layer is called **depletion layer**. It is of the order of 10^{-6} m.

The potential difference produced across the layer is called the **potential barrier**. It is about 0.3 V for germanium junction diode and about 0.7 V for silicon junction diode generally.



Depletion region : It is the region across the p- *n* junction where there are only bound charges. Free charge are not there.

Barrier Potential: The potential which tends to prevent the movement of electron from the n-region into the p-region, is called a barrier potential.The polarity of this potential is such as to oppose further flow of carriers.

(a) (i) The width of depletion layer at *p-n* junction decreases in the forward bias because electric fields across the junction due to barrier potential and external biasing are in opposite direction.

(ii) The width of depletion layer at *p-n* junction increase in the reverse bias because electric fields due to barrier potential and due to external biasing are the same direction.

(b) Increase in doping concentration reduces the width of depletion layer as $V = E_i d$
For a given value of potential barrier, electric field increases and width of depletion region decreases. When doping concentration is high then same value of barrier potential can be achieved with shorter width of depletion region.

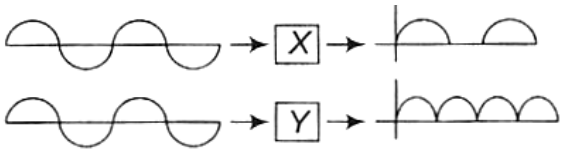
19) What do the terms `depletion region' and 'barrier potential' mean for a p-n junction? [S.P.]

20) Explain how a depletion region is formed in a junction diode? [Delhi 2011]

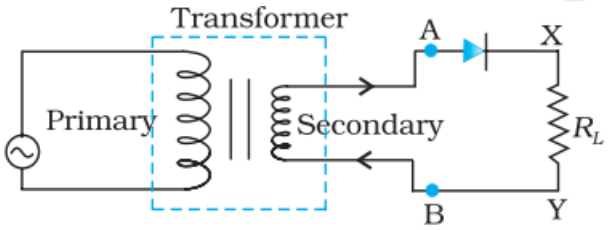
21) Name the important processes that occurs during the formation of a *p-n* junction. Explain briefly, with the help of a suitable diagram, how a *p-n* junction is formed. Define the term 'barrier potential'? [Foreign 2011][All India 2012]

22) An AC signal is fed into two circuits X and Y and the corresponding output in the two cases have the waveforms shown below.

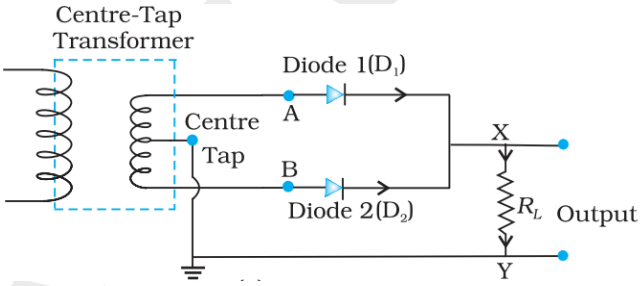
Name the circuits X and Y. Also draw their detailed circuit diagrams[CBSE Sample Papers]



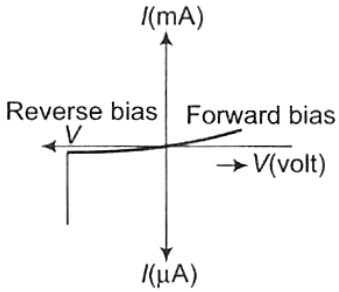
SOL: Circuit X is a half wave rectifier , Circuit Y is a full wave rectifier



Half wave rectifier



Full wave rectifier



23) Draw a labelled diagram of a full wave rectifier circuit. State its working principle. Show the input-output waveforms. [All India 2011] [Foreign 2008]

24) The figure below shows the V -I characteristics of a semiconductor device.

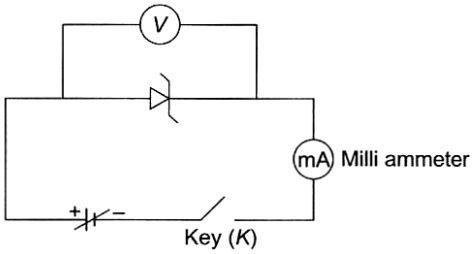
(i) Identify the semiconductor device used here

(ii) Draw the circuit diagram to obtain the given characteristics of this device

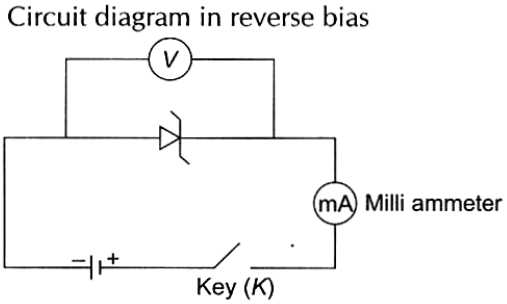
(iii) Briefly explain how this device is used as a voltage regulator? [CBSE Sample Papers]

SOL(i)The given figure shows the V- I characteristics of a zenerdiode.

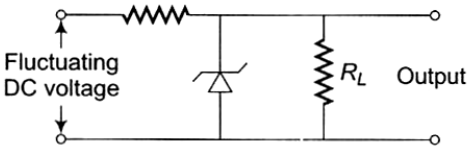
(ii) Circuit diagram in forward bias



Circuit diagram in reverse bias



(iii) Zener diode as a voltage regulator



If a zener diode is reverse biased and is connected to a voltage supply, then after a certain voltage, the current suddenly increases in the zener diode, this increases voltage drop. Due to this property, it can also be used as a voltage regulator.

25) the following table provides the set of values of V and I obtained for a given diode :

	V	I
Forward biasing	2.0 V	60 mA
	2.4 V	80 mA
Reverse biasing	0 V	0 μA
	– 2 V	– 0.25 μA

Assuming the characteristics to be nearly linear, over this range, calculate the forward and reverse bias resistance of the given diode.

SOL: For forward biasing :

$$\Delta V = 2.4 - 2.0 = 0.4 \text{ V} ; \quad \Delta I = 80 - 60 = 20 \text{ mA}$$

$$\therefore \quad r_{fb} = \frac{\Delta V}{\Delta I} = \frac{0.4 \text{ V}}{20 \times 10^{-3} \text{ A}} = \mathbf{20\ \Omega.}$$

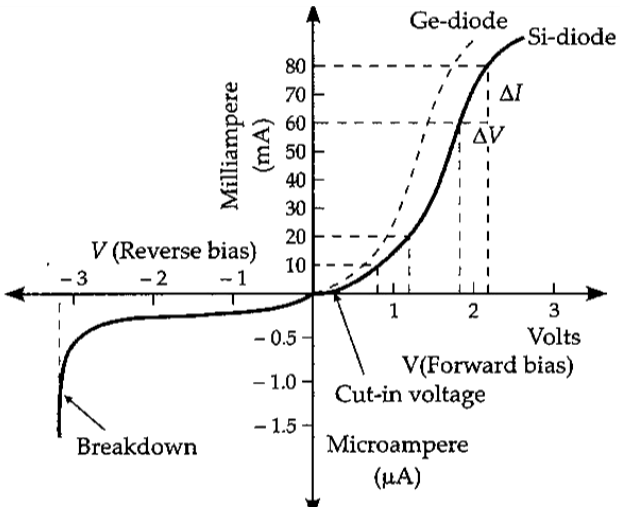
For reverse biasing :

$$\Delta V = -2 - 0 = -2 \text{ V}$$

$$\Delta I = -0.25 - 0 = -0.25 \text{ μA}$$

$$\therefore \quad r_{rb} = \frac{-2 \text{ V}}{-0.25 \times 10^{-6} \text{ A}} = \mathbf{8 \times 10^6\ \Omega.}$$

26) The V-I characteristic of a silicon diode is given in Fig. Calculate the diode resistance in : (a) forward bias at V = ± 2 V and V = + 1 V, and (b) reverse bias V = –1 V and –2 V.



Typical *V-I* characteristics of silicon and germanium diodes.

SOL: (a) The forward bias diode resistance is given by $r_{fB} = \dfrac{\Delta V}{\Delta I}$

where ΔV and ΔT are the small changes in the voltage and current near the desired values.

$$r_{\text{fb}}\,(at + 2\text{ V}) = \frac{(2.2 - 1.8)\text{ V}}{(80 - 60)\text{ mA}} = \frac{0.4\text{ V}}{20 \times 10^{-3}\text{ A}} = \mathbf{200\ \Omega.}$$

$$r_{\text{fb}}\,(at + 1\text{ V}) = \frac{(1.2 - 0.8)\text{ V}}{(20 - 10)\text{ mA}} = \frac{0.4\text{ V}}{10 \times 10^{-3}\text{ A}} = \mathbf{400\ \Omega.}$$

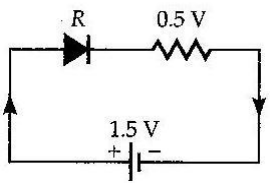
(b) In the reverse bias characteristic, the non-linearity in the *V -I* curve is small. The slopes of *V -I* curve at -1 V and -2 V are nearly equal.

$$r_{\text{rb}}\,(-2\text{ V}) = \frac{-2\text{ V}}{-0.25\,\mu\text{A}} = \frac{2\text{ V}}{0.25 \times 10^{-6}\text{ A}}$$

$$= \mathbf{8 \times 10^{6}\ \Omega.}$$

Also, $\quad r_{\text{rb}}\,(-1\text{ V}) \approx \mathbf{8 \times 10^{6}\ \Omega.}$

27) A p-n junction diode when forward biased has ca drop of 0.5 V which is assumed to be independent of current. The current in excess of 10 mA through the diode produces a large Joule heating which damages (burns) the diode. If we want to use a 1.5 V battery to forward bias the diode, what should be the value of resistor used in series with the diode so that the maximum current does not exceed 5 mA ?



SOL:

Here $V_D = 0.5$ V, $V = 1.5$ V,

$I = 5\text{ mA} = 5 \times 10^{-3}$, $R = ?$

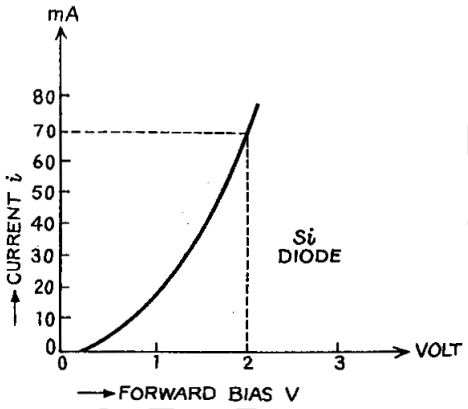
The voltage equation for the diode circuit is

$$IR + V_D = V$$

or $\quad 5 \times 10^{-3}\text{ A} \times R + 0.5\text{ V} = 1.5\text{ V}$

or $\quad R = \mathbf{200\ \Omega.}$

28) The V- *i* characteristic of a silicon diode is given in the figure. Calculate the diode resistance in forward bias at V = + 2 volt,



SOL: *At* forward bias, V = + 2 volt, the diode current i is 70 mA = (70×10^{-3}) A. Therefore, The diode resistance is

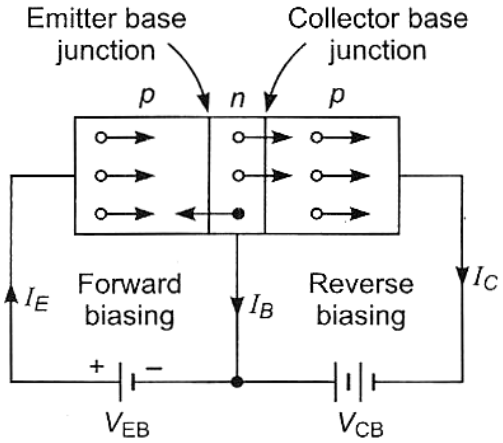
$$R_d = \frac{V}{i} = \frac{2\ \text{V}}{(70 \times 10^{-3})\ \text{A}}$$

$$= 28{\cdot}57\ \Omega\ .$$

Transistor Questions (Pg No. 66)

1) Describe briefly with the help of a circuit diagram, how the flow of current carriers in a *p-n-p* transistor is regulated with emitter-base junction forward biased and base-collector junction reverse biased. [All India 2012]

SOL: Heavily doped emitter is subjected to electric field by emitter-base battery and consequently holes gets drifted towards collector through thin and lightly doped base region. Nearly 5% hole, which drifted from emitted combined with electron in base region and remaining nearly 95% hole reaches collector under the influence V_{CE}.



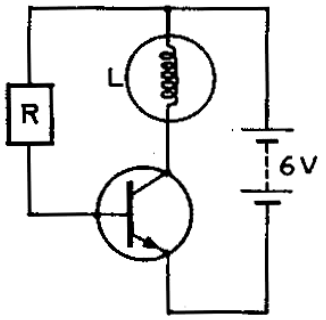
2) Write the function of base region of a transistor. Why is this region made thin and slightly doped?

ANS: The base controls the flow of majority charge-carriers (holes in *p-n-p* and electrons in *n-p-n* transistors) from the emitter to the collector. It is made very thin (compared with emitter and collector) and is lightly doped to have very small number of free electrons (in case of *p-n-p)* or holes (in case of *n-p-n) in* it. This minimises the recombination of holes and electrons in it. Most (about 98%) of the holes, or electrons, arriving from the emitter diffuse across the base and reach the collector. Hence, the collector-current is almost equal to the emitter-current, the base-current being comparatively much smaller. This is the main reason of power-gain and voltage-gain obtained by a transistor. If the base region were made quite thick and heavily doped, then most of the charge carriers coming from the emitter would have been neutralised in the base by recombination and there would be little collector-current and the very purpose of the transistor would be defeated.

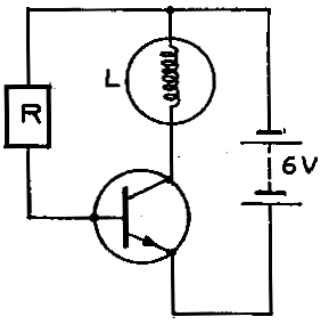
3) If the base region of a transistor is made large, as compared to a usual transistor, how does it affect (i) the collector current, and (ii) current gain of this transistor ?

ANS: The collector-current and current-gain both decrease.

4) In only one of the circuits given below, the lamp *L* lights. Which circuit is it ? Give reason for your answer.



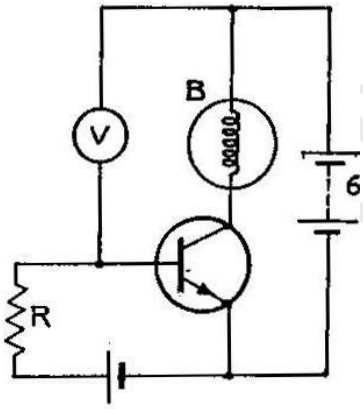
(a)



(b)

Ans. In circuit (a) only, the emitter of the *n-p-n* transistor is forward-biased *and* the collector is reverse-biased. So the lamp *L* lights up in case (a).

5) In the given circuit, a voltmeter *V* is connected across a bulb *B* . What changes would occur at bulb *B* and voltmeter *V* , if the resistance *R* is reduced. Give reason for your answer.



ANS: The transistor is of *n-p-n* type. If the resistance *R* is reduced, the forward bias increases, and so the base-current and also the collector-current increases. The bulb glows brightly and the voltmeter shows a higher voltage.

6) What is the phase difference between the input and out put signals of common phase amplifiers?

ANS: 180^0

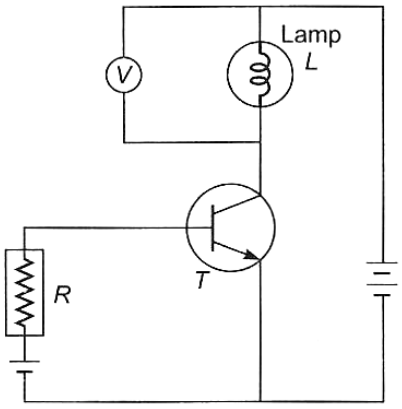
7) Would you prefer to use a transistor amplifiers in common- base configuration or in common –emitter configuration? Why?

ANS: common emitter configuration is preferred because it give both current gain and voltage- gain and hence a much higher power –gain. Common base gives a small current loss.

8) **For a common –emitter amplifier , the current gain is 69 . If the emitter current is 7.0 mA , calculate the collector and the base currents.**

ANS: 6.9mA,0.1mA

9) In the given circuit, a voltmeter V is connected across lamp *L*. What changes would you observe in the lamp *L* and the voltmeter, if the value of resistor *R* is reduced? [Delhi 2011C]



SOL: Lamp glows brighter and voltmeter reading increases with the decrease of *R.* Input current increase which in turn by transistor action lead to increase collector current. This makes lamp brighter and hence, voltmeter reading goes up.

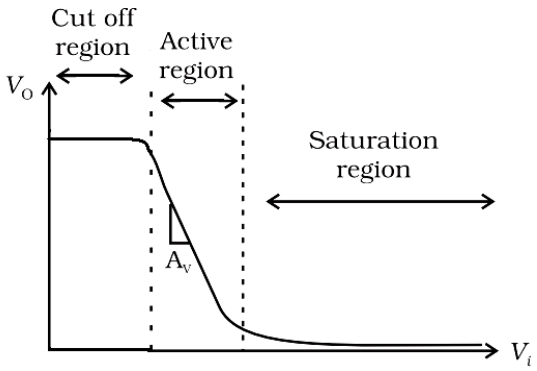
10) A student has to study the input and output characteristics of a n-p-n silicon transister in the Common Emitter configuration. What kind of a circuit arrangement should she use for this purpose? Draw the typical shape of input characteristics likely to be obtained by her. What do we understand by the cut off, active and saturation states of the transistor? [S.P.]

SOL: Cut off state: Transistor will be in cut off state when output current (I_C) is zero. (input voltage is minimum = 0.6 V for Si)Transistor does not conduct.
Active state: When there is some current in collector-emitter circuit transistor is said to be active state. (for Si it is for voltage greater than 0.6 V).
Saturation state : When output voltage tends to zero. Transistor is said to be in saturation state.

11) (a) Draw the circuit for studying the input and output characteristics of and transistor in CE configuration. Show, how, from the output characteristics, the information about the current amplification factor β_{AC} can obtained.

(b) Draw a plot of the transfer characteristics *(V_o versus V_i)* for a base-biased transistor in CE configuration. [Foreign 2012]

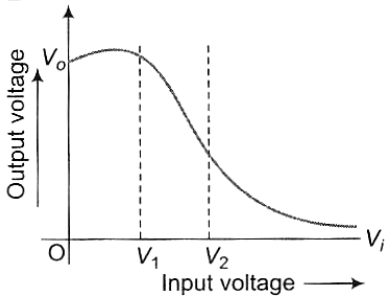
SOL: (b) Transfer characteristics curve, for a base-biased transistor in CE configuration.



12) Draw the transfer characteristics of a base biased transistor in its common emitter configuration. Explain briefly the meaning of the term 'active region' in these characteristics. For what practical use, do we use the transistor in this 'active region'? [S.P.]

SOL: In case of transistor there is a minimum value of input voltage (V_i) below which it remains in cut off state. For Si-transistor it is 0.5 to 0.7 V. When $V_i > 0.7$ volt, the transistor conducts and there is some current (I_c.) in collector-emitter circuit. Under this condition the transistor is said to be in active state. Transistor is used in active state in case of amplifier circuit.

13) The transfer characteristic of a base biased transistor in CE configuration is as shown. Name the region corresponding to the values (i) 0 to V_1 (ii) V_1 to V_2 (iii) greater than V_2 of the input voltage applied to the transistor. What is the practical use of transistor, when it is operated in this voltage range? Name the source that results in a higher energy of the output of a transistor operated in this range?



[CBSE Sample Papers]

SOL:

(i) 0 to V_1 region is cut-off region

(ii) V_1 to V_2 region is active region

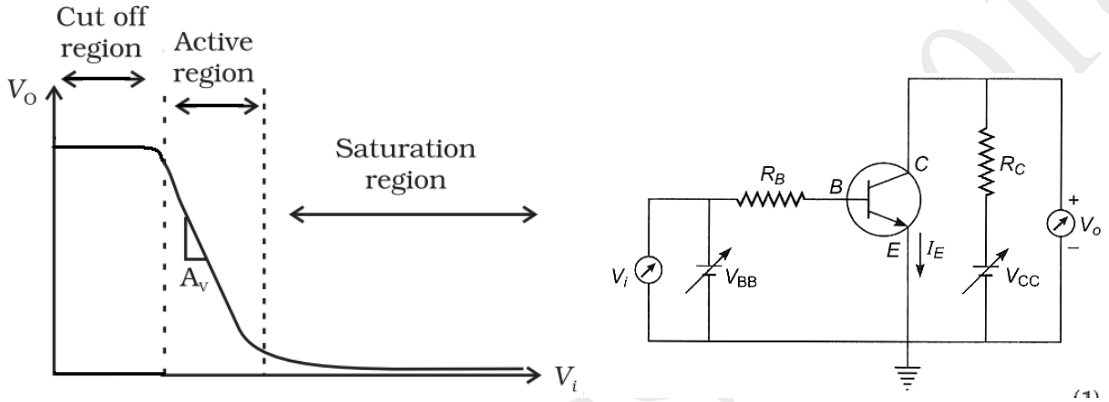
(iii) greater than V_2 region is saturation region

Transistor works as an amplifier in the active region (V_1 to V_2).

The energy for the higher AC power at the output is supplied by the biasing battery.

14) Draw the transfer characteristic curve of a base biased transistor in CE configuration. Explain clearly how the active region of the V_o *versus* V_i curve in a transistor is used as an amplifier. [Delhi 2011]

SOL: The transfer characteristic curve of base biased transistor in CE configuration are shown below



As V_i increases slightly above 0.6 V, a current I_C flows in the output circuit and the transistor arrives in active state.

$$V_o = V_{CC} - I_C R_C$$

with the growth of I_c, V_c decrease linearly. Also, voltage gain in active state is given by

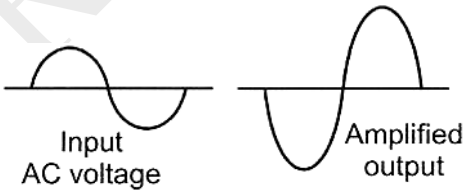
$$A_V = -\frac{\Delta V_o}{\Delta V_i}$$

$$\Delta V_o > \Delta V_i$$

There is voltage gain and hence amplification of voltage takes place. Thus, transistor used as an amplifier.

15) Give a circuit diagram of a common emitter amplifier using an *n-p-n* transistor. Draw the input and output waveforms of the signal. Write the expression for its voltage gain. [All India 2010]

SOL:



Voltage gain It is equal to the ratio of small change in output voltage at collector to that of change in input voltage i.e.,

$$A_V = \frac{Output\ Voltage}{Input\ Voltage} = \frac{\Delta V_o}{\Delta V_i} = \frac{\Delta I_C R_o}{\Delta I_B R_{in}}$$

$$A_V = \beta_{ac} \times \frac{R_o}{R_{in}}$$

Voltage gain = β_{ac} × Resistance gain , where, β_{AC} is AC current gain.

16) Draw the circuit diagram of a common emitter amplifier using *n-p-n* transistor. What is the phase difference between the input signal and output voltage? State two reasons why a common emitter amplifier is preferred to a common base amplifier. [All India 2007]

SOL: *Phase relation of 180° (opposite phase) waveform.*

Reasons behind preference of CE over CB amplifier.

1. The current gain in common emitter amplifier (β) is greater than the current gain in common base (α) amplifier i.e., $\beta > \alpha$.
2. The phase relation between output and input signals in CE amplifier are in opposite phase whereas in CB amplifier are in same phase.

17) Draw a simple circuit of a CE transistor amplifier. Explain its working. Show that the voltage gain, A_V, of the amplifier is given by $A_v = \frac{\beta_{AC} R_L}{r_i}$ where, β_{AC} is the current gain, R_L is the load resistance and r_i , is the input resistance of the transistor. What is the significance of the negative sign in the expression for the voltage gain.

SOL: The output voltage of CE amplifier differ in phase from the input voltage by 180° or π or in opposite phase is represented by negative sign.

$$A_V = -\beta_{ac} \times \frac{R_L}{R_i}$$

18) Draw the labelled circuit diagram of a common-emitter transistor amplifier. Explain clearly how the input and output signals are in opposite phase? [All India 2008]

SOL: Relationship between input and output signal of *n-p-n* transistor amplifier, When positive half cycle is fed into input circuit, forward bias of emitter base circuit decreases. This lead to decrease I_E and by transistor action, collector current decreases. Since, output voltage

$V_o = V_{CE} - I_C R_C$, therefore decrease in collector current, increases output voltage. As the collector is connected with the negative terminal of battery V_{cc}, the increase it collector voltage imply that negatively of collector increases. Thus, corresponding tc positive half cycle of input AC a negative amplified cycle is obtained at collector and *vice-versa.* This shows that output and input signals are in opposite phase.

19) Draw transfer characteristics of a common emitter *n-p-n* transistor. Point out the region in which the transistor operates as an amplifier.

Define the following terms used in transistor amplifiers :

(a) Input resistance
(b) Output resistance
(c) Current amplification factor. [Foreign 2011] [All India 2011C]

SOL: The active region of transfer characteristic curve operates as an amplifier.

(a) The input resistance r_i of tansistor in CE configuration is defined as the ratio of small change in base-emitter voltage to the corresponding small change in the base current, when the collector emitter voltage is kept constant i.e.,

$$r_{in} = \left(\frac{\Delta V_{BE}}{\Delta I_B} \right)_{V_{CE}}$$

(b) **Output resistance**: The ratio of variation of collector emitter voltage (V_{CE}) and corresponding change in collector current (ΔI_c) when base current remains constant, is called output characteristic curve.

$$r_O = \left(\frac{\Delta V_{CE}}{\Delta I_C} \right)_{I_B}$$

(c) The current amplification factor of ac transistor in CE configuration is equal to the ratio of the small change in the collector current (ΔI_C) to the small change in base current (I_B) when collector-emitter voltage is kept constant *i.e.*.

$$\beta_{ac} = \left(\frac{\Delta I_C}{\Delta I_B} \right)_{V_{CE}}$$

20) Draw the general shape of the 'transfer characteristics' of a transistor in its CE configuration. Which regions of this characteristic of a transistor, are used when it works as an amplifier? [All India 2010C]

SOL: The **active region** of transfer characteristic curve is used as an amplifier.

21) Draw the labelled circuit diagram of a common-emitter transistor amplifier. Explain clearly how the input and output signals are in opposite phase? [All India 2008]

SOL: Relationship between input and output signal of *n-p-n* transistor amplifier, When positive half cycle is fed into input circuit, forward bias of emitter base circuit decreases. This lead to decrease I_E and by transistor action, collector current decreases. Since, output voltage $V_o = V_{CE} - I_C R_C$, therefore decrease in collector current, increases output voltage. As the collector is connected with the negative terminal of battery V_{CC}, the increase it collector voltage imply that negatively of collector increases. Thus, corresponding to positive half cycle of input AC a negative amplified cycle is obtained at collector and *vice-versa.* This shows that output and input signals are in opposite phase.

22) The AC current gain of a transistor is 120. What is the change in the collector current in the transistor whose base current changes by 100 μ A? [All India 2006C]

SOL:

$\because$ Current gain $\beta = \dfrac{\Delta I_C}{\Delta I_B}$

$$120 = \frac{\Delta I_C}{(100\ \mu A)}$$

$$\Delta I_C = 120 \times 100\ \mu A = 12\ mA.$$

23) Draw a circuit diagram for use of *n-p-n* transistor as an amplifier in common emitter configuration. The input resistance of a transistor is 1000 Ω . On changing is base current by 10 μA, the collector current increases by 2 mA. If a load resistance of 5 kΩ is used in the circuit, calculate

(a) The current gain

(b) Voltage gain of the amplifier. [Delhi 2006]

SOL: $R_i = 1000\ \Omega$, $\Delta I_B = 10\ \mu A = 1\times 10^{-5} A$, $\Delta I_C = 2mA = 2\times 10^{-3} A$, $R_L = 5k\Omega = 5\times 10^3 \Omega$

(a) The current $\beta_{ac} = \left(\dfrac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}} = \dfrac{2\times 10^{-3}}{1\times 10^{-5}} = 2\times 10^2 = 200$

(b)Voltage Gain $A_V = \beta_{ac} \times \dfrac{R_L}{R_{in}} = 200 \times \dfrac{5\times 10^3}{1000} = 1000$

24) For a transistor connected in common emitter mode, the voltage drop across the collector is 2 V and β is 50. Find the base current, if R_C is 2 KΩ.

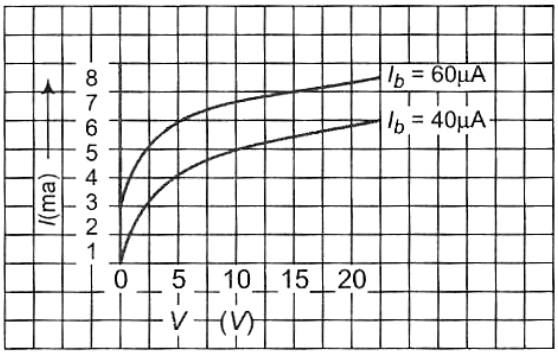
SOL: Here $V_{CE} = 2V$, $\beta = 50$, $R_C = 2K\Omega = 2\times 10^{-3}$ A = 1 mA

$$\therefore \quad I_C = \frac{V_{CE}}{R_C} = \frac{2}{2\times 10^3} = 10^{-3}\ A = \mathbf{1\ mA.}$$

$$\text{As} \quad \beta = \frac{I_C}{I_B}$$

$$\therefore \quad I_B = \frac{I_C}{\beta} = \frac{10^{-3}}{50}\ A = \mathbf{20\ \mu A}.$$

25) A certain *n-p-n* transistor has the common emitter output characteristics as shown



(a) Find the emitter current at V_{CC} =10 V and I_b = 60 μ A

(b) Find β at this point. [CBSE Sample Papers]

SOL:

(a) Given, $V_{cc} = 10$ V and $I_b = 60\ \mu A$

From the figure,

When $I_b = 60\ \mu A$

Then, $I_c = 6$ mA

So, emitter current

$$I_e = I_c + I_b$$
$$= 60\ \text{mA} + 60\ \mu\text{A}$$
$$= 6\ \text{mA} + 60 \times 10^{-3}\ \text{mA}$$
$$= 6\ \text{mA} + 0.06\ \text{mA}$$
$$I_e = 6.06\ \text{mA}$$

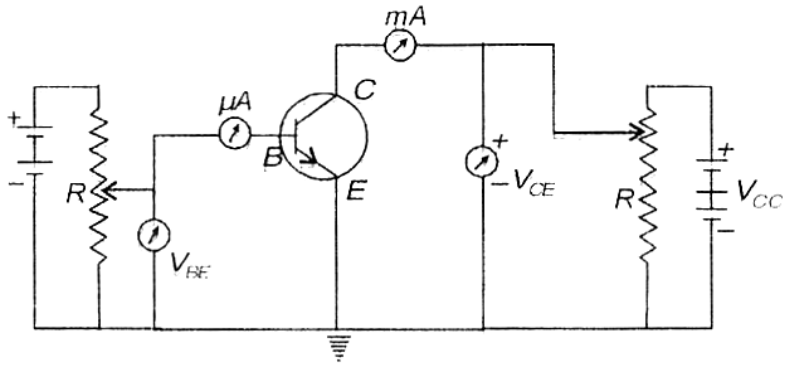
(b) Current amplification factor (β)

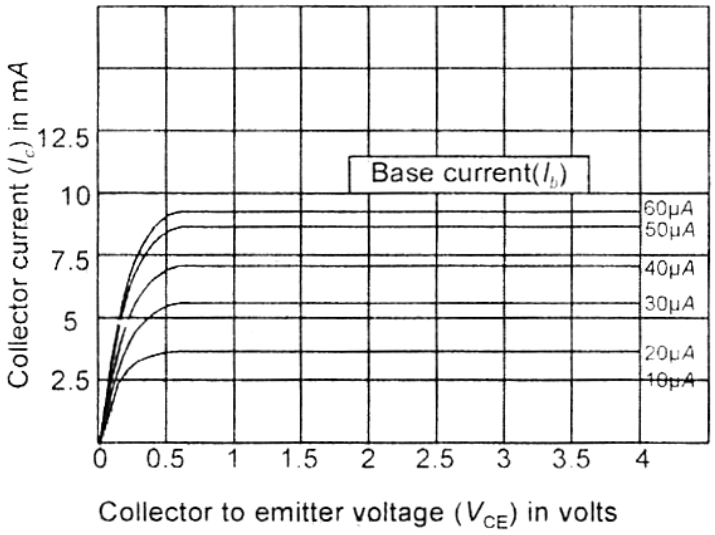
$$= \frac{\Delta I_c}{\Delta I_b}$$
$$= \frac{6\ \text{mA}}{60\ \mu\text{A}}$$
$$= \frac{6\ \text{mA}}{60 \times 10^{-3}\ \text{mA}}$$
$$= \frac{6}{6 \times 10^{-2}}$$
$$\beta = 100$$

26) The given circuit diagram shows a transistor configuration along with its output characteristics. Identify

(i) the type of transistor used and

(ii) the transistor configuration employed.





Use these graphs to obtain the approximate value of current amplification factor for the transistor at V_{CE} = 3V. [S.P.]

SOL: *(i) n-p-n* transistor *(ii)* common emitter configuration

(iii) Current amplification factor $\beta_{ac} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}$

We take characteristics for any two values of I_B . Then at V_{CE} =3V we find out values of I_C from the graph. Here we take ΔI_B = (40–20)μ A = 20 μ A

ΔI_C = (7–4)m A = 20 m A

Therefore, $\beta = \frac{3\times10^{-3}}{20\times10^{-6}} = 150$

27) The current gain for common-emitter amplifier is 59. If the emitter-current is 6.0 mA, find (i) base-current, and (ii) collector-current.

SOL: The d.c. current gain in common- emitter transistor circuit is given by

$$\beta\,(\text{d.c.}) = \frac{i_C}{i_B}.$$

Here $\beta = 59$. $\therefore \frac{i_C}{i_B} = 59.$ ...(i)

Now, the sum of base-current i_B and collector-current i_C equals the emitter-current i_E, that is,

Now, the sum of base-current i_B and collector-current i_C equals the emitter-current i_E, that is,

$$i_B + i_C = i_E = 6{\cdot}0\text{ mA} \quad \text{(given)}. \qquad \text{...(ii)}$$

Solving eq. (i) and (ii), we get

$$i_B = 0{\cdot}1\text{ mA} \text{ and } i_C = 5{\cdot}9\text{ mA}.$$

28) A common-emitter transistor amplifier has a current gain of 50. The collector resistance is 5 $k\Omega$ and the input resistance is 1 $k\Omega$, calculate the output voltage if input voltage is 0.01 V.

SOL:

In common-emitter amplifier, the voltage gain is given by

$$A_V = \beta\,(\text{a.c.}) \times \frac{R_{out}}{R_{in}},$$

where R_{out} is the output resistance (here R_{out} = collector resistance) and R_{in} is the input resistance of the circuit.

$$\therefore \quad A_V = 50 \times \frac{5\ \text{k}\Omega}{1\ \text{k}\Omega} = 250.$$

$$\text{Output voltage} = A_V \times \text{input voltage}$$
$$= 250 \times 0{\cdot}01\ \text{V} = \mathbf{2{\cdot}5\ V.}$$

29) The input resistance of a silicon transistor is 665 Ω . Its base-current is changed by 15 μA which results in a change of 2 mA in the collector-current. The transistor is used as a common-emitter amplifier with a load resistance of 5 $k\Omega$. What is the voltage gain of the amplifier ? Also calculate the transconductance of the transistor.

SOL:

The alternating current gain β of a common-emitter amplifier is defined by

$$\beta\,(\text{a.c.}) = \frac{\Delta i_C}{\Delta i_B},$$

where Δi_C and Δi_B are the changes in collector-current and base-current respectively. Thus

$$\beta = \frac{2\ \text{mA}}{15\ \mu\text{A}} = \frac{2 \times 10^{-3}\ \text{A}}{15 \times 10^{-6}\ \text{A}} = 133{\cdot}3.$$

Now, the a-c voltage gain of a common-emitter amplifier is given by

$$A_V = \beta \times \frac{R_{out}}{R_{in}}.$$

Here, output resistance R_{out} = 5 kΩ = 5000 Ω and input resistance R_{in} = 665 Ω.

$$\therefore \quad A_V = 133{\cdot}3 \times \frac{5000\ \Omega}{665\ \Omega} \simeq \mathbf{1000.}$$

Now, the transconductance of the transistor is defined as

$$g_m = \frac{\Delta i_C}{\Delta V_{BE}},$$

where ΔV_{BE} is change in base-to-emitter voltage. Further, the input resistance is given by

$$R_{in} = \frac{\Delta V_{BE}}{\Delta i_B}.$$

From the last two equations, we have

$$g_m \times R_{in} = \frac{\Delta i_C}{\Delta i_B} = \beta\,(\text{a.c.})$$

or

$$g_m = \frac{\beta\,(\text{a.c.})}{R_{in}} = \frac{133{\cdot}3}{665\ \Omega} = \mathbf{0{\cdot}2\ \Omega^{-1}}.$$

30) A change of 0.2 mA in base-current causes a change of 5 mA in the collector-current for a common-emitter amplifier. (i) Find the a-c current gain of the transistor. (ii) If the input resistance is 2 $k\Omega$) and its voltage gain is *75*, calculate the load resistor used in the circuit.

SOL:

(i) By definition, the alternating-current gain β is given by

$$\beta\,(\text{a.c.}) = \frac{\Delta i_C}{\Delta i_B} = \frac{5 \times 10^{-3}\,\text{A}}{0{\cdot}2 \times 10^{-3}\,\text{A}} = 25.$$

(ii) Voltage-gain, $A_V = \beta\,(\text{a.c.}) \times \frac{R_{out}}{R_{in}}$.

$$\therefore\ R_{out} = \frac{A_V \times R_{in}}{\beta\,(\text{a.c.})} = \frac{75 \times 2\,\text{k}\Omega}{25} = \mathbf{6\,k\Omega}.$$

31) In a transistor, the base-current-is changed by 10 μA. This results in a change of 0.01 V in base to emitter voltage, and a change of 1.0 mA in the collector-current. Find : (i) the current gain β (a-c) and (ii) the transconductance g_m If this transistor is used as an amplifier with load resistance 5 $k\Omega$ Calculate the voltage gain of the amplifier.

SOL:

The transconductance is related to alternating-current gain by

$$g_m = \frac{\beta\,(\text{a.c.})}{R_{in}},$$

where R_{in} is input resistance.

$$\therefore\ R_{in} = \frac{\beta\,(\text{a.c.})}{g_m} = \frac{100}{0{\cdot}1\ \Omega^{-1}} = 1000\,\Omega = 1\,\text{k}\Omega.$$

By definition, the voltage gain is

$$A_V = \beta\,(\text{a.c.}) \times \frac{R_{out}}{R_{in}}$$
$$= 100 \times \frac{5\,\text{k}\Omega}{1\,\text{k}\Omega} = \mathbf{500}.$$

(i) By definition, the alternating-current gain β is given by

$$\beta\,(\text{a.c.}) = \frac{\Delta i_C}{\Delta i_B} = \frac{1{\cdot}0\,\text{mA}}{10\,\mu\text{A}} = \frac{1{\cdot}0 \times 10^{-3}\,\text{A}}{10 \times 10^{-6}\,\text{A}} = \mathbf{100}.$$

(ii) The transconductance of the transistor is defined by

$$g_m = \frac{\Delta i_C}{\Delta V_{BE}}.$$

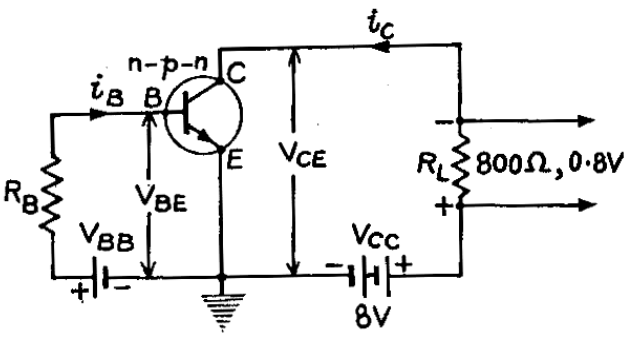
Here $\Delta i_C = 1{\cdot}0\,\text{mA} = 1{\cdot}0 \times 10^{-3}\,\text{A}$ and $\Delta V_{BE} = 0{\cdot}01\,\text{V}$.

$$\therefore\ g_m = \frac{1{\cdot}0 \times 10^{-3}\,\text{A}}{0{\cdot}01\,\text{V}} = \mathbf{0{\cdot}1\ mho\ (\Omega^{-1})}.$$

32) An *n-p-n* transistor is connected in common-emitter configuration in which collector supply is 8 V and the voltage-drop across the load-resistance of 800 Ω connected in the collector circuit is 0.8 V. If current amplification factor is 25, determine collector-emitter voltage and base-current. If the input resistance of the transistor is 200 Ω , calculate the voltage-gain and power-gain.

SOL:

A common-emitter *n–p–n* amplifier circuit is shown in the diagram. V_{CC} and V_{BB} are the collector-supply and base-supply voltages respectively and R_L is the load-resistance in the collector circuit.



The collector-current is

$$i_C = \frac{\text{voltage-drop across } R_L}{R_L}$$

$$= \frac{0{\cdot}8\ \text{V}}{800\ \Omega} = 1{\cdot}0 \times 10^{-3}\ \text{A}.$$

The collector-emitter voltage is

$$V_{CE} = V_{CC} - i_C R_L = 8\ \text{V} - 0{\cdot}8\ \text{V} = \mathbf{7{\cdot}2\ V}.$$

Now, the current-gain in common-emitter configuration is

$$\beta = 25 \text{ (given)}.$$

But β (d-c) $= i_C / i_B$. Therefore, the base current is

$$i_B = \frac{i_C}{\beta} = \frac{1{\cdot}0 \times 10^{-3}\ \text{A}}{25} = 0{\cdot}04 \times 10^{-3}\ \text{A} = \mathbf{40\ \mu A}.$$

The voltage-gain is

$$A_V = \beta\left(\frac{R_L}{R_B}\right) = 25 \times \left(\frac{800\ \Omega}{200\ \Omega}\right) = \mathbf{100}.$$

The power-gain (voltage-gain × current-gain) is

$$A_P = A_V \times \beta = 100 \times 25 = \mathbf{2500}.$$

33) Draw typical output characteristics of an *n-p-n* transistor in CE configuration. Show how these characteristics can be used to determine output resistance.[All India 2013]

PRACTICE QUESTIONS (Logic Gates) Pg. 92

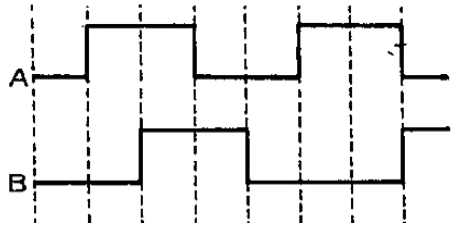
1) Why are the NAND and NOR logic gates called digital building blocks ?

ANS: The repeated use of NAND, or NOR, gate can produce all the three basic gates (OR, AND and NOT) whose different combinations provide us a large number of digital circuits. Hence NAND and NOR gates are called 'digital building blocks'.

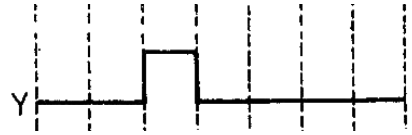
2) Draw a logic circuit diagram showing how a NAND gate can be converted into NOT gate.

ANS: If the two inputs of a NAND gate are joined together to make one input, then the NAND gate acts as a NOT gate.

3) Sketch the output waveform from an AND gate for the inputs A and B shown in the figure.



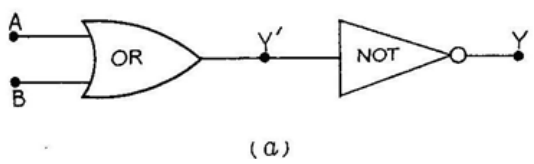
SOL:



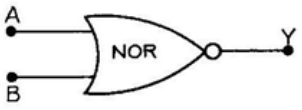
4) The output of a 2-input NOR gate is fed into a NOT gate. Draw the logic circuit of this combination of gates and write the truth table for the output of the combination for all inputs. [Foreign 2007]

5) The output of a 2-input OR gate is fed to a NOT gate. Name the new gate obtained. Draw the logic circuit of the combination of gates. Give its logic symbol and write down its truth table

ANS: The combination of OR and NOT gates is a NOR gate. The logic circuit of the combination and the logic symbol of the resulting NOR gate are drawn in Fig. (a) and (b) respectively



(a)



(b)

A	B	Y′(=A+B)	Y(= $\overline{A+B}$ =$\overline{Y'}$)
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

(a)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

NOR

(b)

6) The output of an OR gate is connected to both the inputs of a NAND gate. Draw the logic circuit of this combination and write its truth table. [Delhi 2007]

7) The output of a 2-input NOR gate is fed as the input to a NOT gate. Name the new logic gate obtained and write down its truth table.

SOL: *Let* us combine the truth tables of NOR and NOT gates, as shown.

INPUTS		OUTPUT OF NOR GATE	OUTPUT OF NOT GATE
A	B	Y′(=$\overline{A+B}$)	Y(=$\overline{Y'}$)
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Columns *A* , *B* and Y form the truth table of the combination. It is the table of OR gate. Hence the new gate is OR gate.

8) Identify the gate shown in the figure. Explain with the help of a circuit diagram?

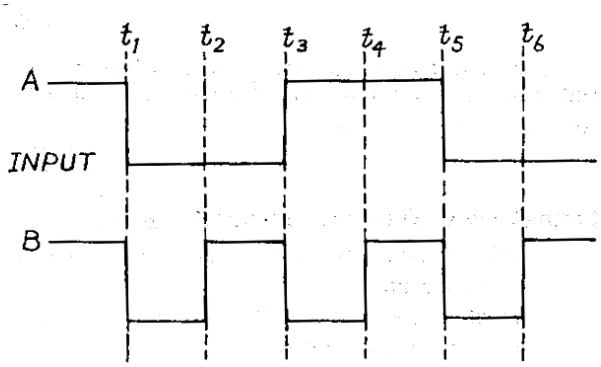
9) (a) The given inputs A and *B* are fed to a 2-input NAND gate. Draw the output waveform of the gate.

SOL: For the NAND gate . the Boolean expression is

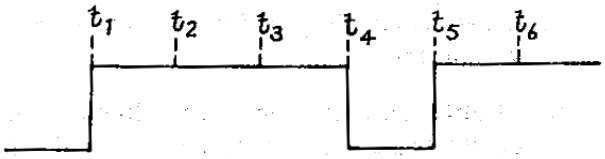
$$Y = \overline{A \bullet B}$$

For the given waveform we have the following values of *A* , *B* and *Y* .

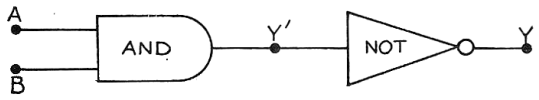
For time $t < t_1$: $A = 1$, $B = 1$ $\Rightarrow Y = 0$
For time t_1 to t_2 : $A = 0$, $B = 0$ $\Rightarrow Y = 1$
For time t_2 to t_3 : $A = 0$, $B = 1$ $\Rightarrow Y = 1$
For time t_3 to t_4 : $A = 1$, $B = 0$ $\Rightarrow Y = 1$
For time t_4 to t_5 : $A = 1$, $B = 1$ $\Rightarrow Y = 0$
For time t_5 to t_6 : $A = 0$, $B = 0$ $\Rightarrow Y = 1$
For time t_6 to t_7 : $A = 0$, $B = 1$ $\Rightarrow Y = 1$.



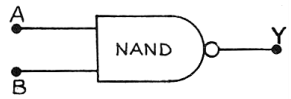
Thus the waveform for out put Y is given in the adjoining diagram.



(b) **The following figure shows the input wavefroms (A, B) and the output waveform (Y) of a gate. Identify the gate, write its truth table and draw its logic symbol.**



SOL: It is a NAND gate,

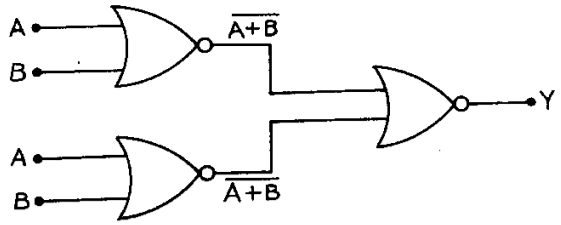


Truth Table

Time interval	Input		Output
	A	B	Y
$t < t_1$ *i.e.*, 0 – 1	1	1	0
1 – 2	0	0	1
2 – 3	0	1	1
3 – 4	1	0	1
4 – 5	1	1	0
5 – 6	0	0	1
6 – 7	0	1	1

10) If the output of a 2 input NOR gate is fed as both inputs A and B to another NOR gate, write down a truth table to find the final output for all combinations of A , B .

SOL: The required circuit is

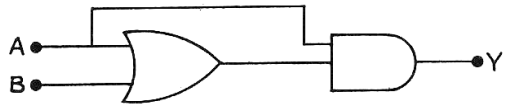


A	B	$\overline{A+B}$	$\overline{A+B}+\overline{A+B}$	$Y=\overline{\overline{A+B}+\overline{A+B}}$
0	0	1	1	0
0	1	0	0	1
1	0	0	0	1
1	1	0	0	1

Hence the logic gate works like OR gate

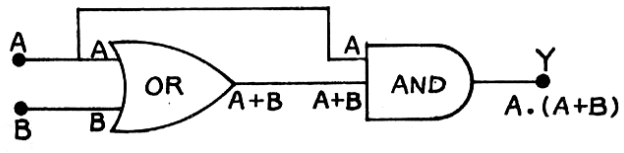
Y= A+B

11) Write the truth table tor the following combination of gates.



SOL:

Let us redraw the given combination, pointing out that the first gate is OR gate and the second gate is AND gate. The inputs of the OR gate are A and B, and its output is $A + B$, that is, A OR B.

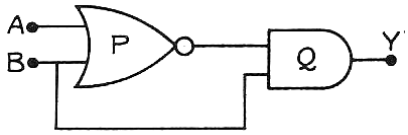


INPUTS		A + B	Y = A.(A+B)
A	B		
0	0	0	0
0	1	1	0
1	0	1	1
1	1	1	1

The inputs of the AND gate are A and $A + B$, and its output is $A \bullet (A + B)$, that is, A AND (A OR B). The truth table for the output $Y = A \bullet (A + B)$ has been derived, using the truth tables of OR and AND gates.

12) Identify the logic gates marked *P* and *Q in* the given logic circuit. Write down outputs at Y for the inputs

(i) A = 0 , *B = 0, (ii) A =1 , B = 1* .

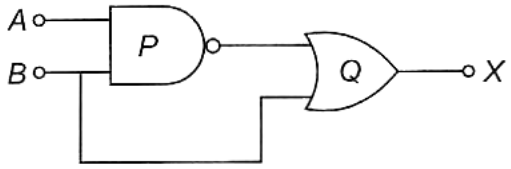


SOL: P is NOR gate, Q is AND gate.

The outputs at Y for $A = 0, B = 0$ and for $A = 1, B = 1$ are 0, 0, as shown in the truth table.

INPUTS		OUTPUT OF NOR GATE	OUTPUT OF AND GATE
A	B	$Y'(=\overline{A+B})$	$Y(=B \cdot Y')$
0	0	1	0
1	1	0	0

13) (a) Identify the logic gates marked P and Q in the given logic circuit.
(b) Write down the output at X for the inputs A = 0, *B* = 0 and A =1, *B* = 1. [All India 2010]



SOL: (a) *P :* NAND gate.

Q : OR gate.

(b) $X = \overline{A \cdot B} + B$

For $A = 0, B = 0, X = \overline{0.0} + 0 = 1 + 0 = 1$

For $A = 1, B = 1, X = \overline{1.1} + 1 = 0 + 1 = 1.$

14) Name the 2-input logic gate, whose truth table is as given. If this logic gate is connected to a NOT gate, what will be the outputs, when (i) A = 0 , B = 0 ,(ii) A = 1 , B = 1 .

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

SOL: NOR gate

On connecting the given gate with NOT gate,

A	B	OUTPUT OF NOR GATE	OUTPUT OF NOT GATE
0	0	1	0
1	1	0	1

15) The truth table gives the output of a 2-input logic gate : (i) Identify the logic gate, and draw its logic symbol. (ii) If the output of this gate is fed as input to a NOT gate, name the new logic gate formed.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

SOL:

(i) It is a NAND gate. Its logic symbol is drawn here.

(ii) The output of NAND gate is fed as input to a NOT gate. We combine the truth tables of NAND and NOT gates, as shown.

Columns A, B and Y form the truth table of the combination. It is the table of AND gate. Thus, the new gate is an AND gate.

INPUTS		OUTPUT OF NAND GATE	OUTPUT OF NOT GATE
A	B	$Y'(=\overline{A \cdot B})$	$Y(=\overline{Y'})$
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

16) What will be the values of inputs A and *B* for the Boolean expression $(\overline{A+B}).(\overline{A.B})=1$? [Delhi 2007]

SOL: $(\overline{A+B}).(\overline{A.B})=1$

Given, $(\overline{A+B})\cdot(\overline{A\cdot B})=1$.

LHS, $(\overline{A+B})\cdot(\overline{A\cdot B})$

If $A=0,\ B=0,$ then $(\overline{0+0})\cdot(\overline{0\cdot 0})=(\overline{0})\cdot(\overline{0})$

$=1$ RHS

Hence, the values of input $A=B=0$.

A	**B**	$(\overline{A+B})$	$(\overline{A.B})$	$(\overline{A+B}).(\overline{A.B})$
0	0	1	1	1
0	1	0	1	0
1	0	0	1	0
1	1	0	0	0